FIG.1

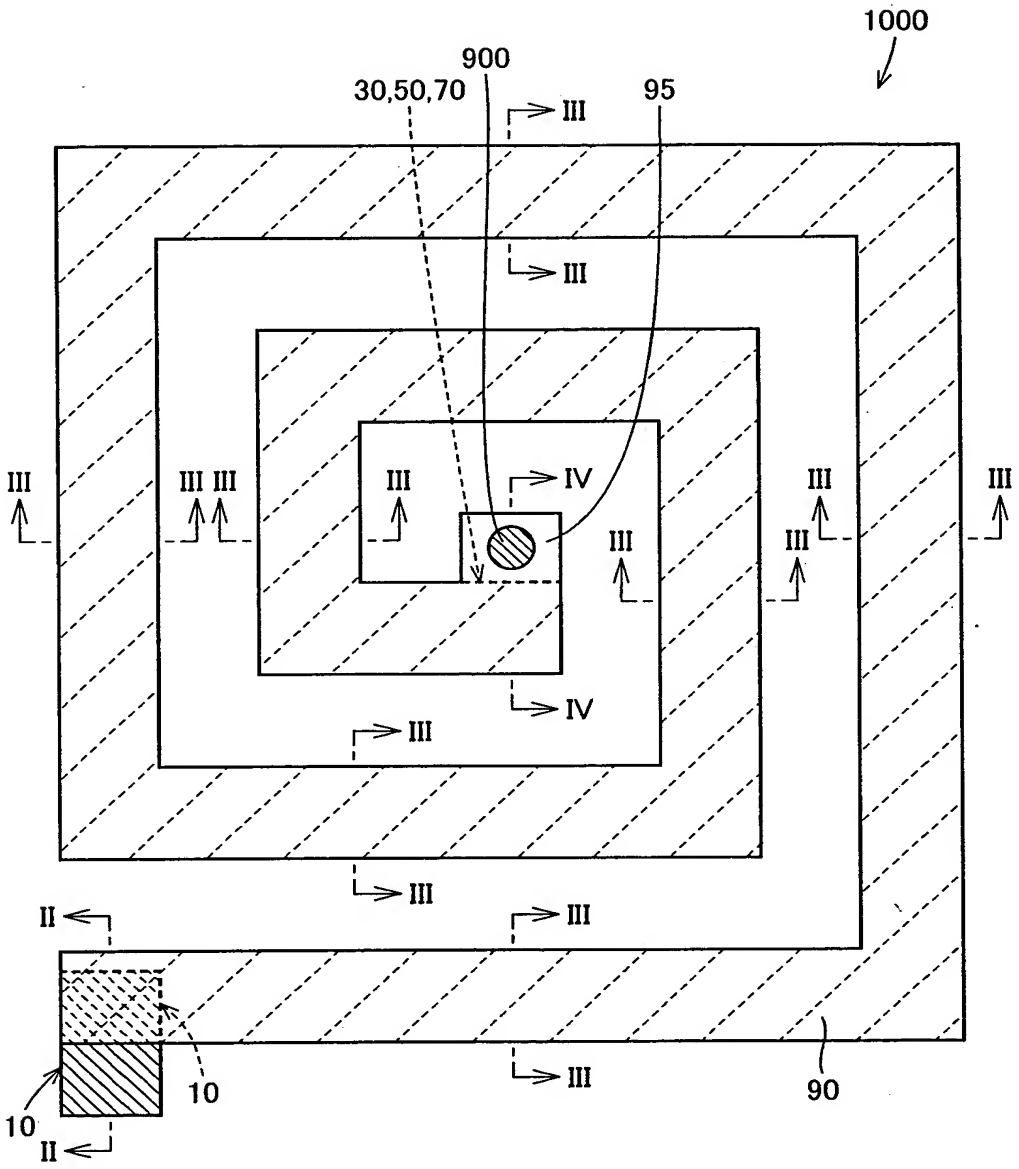

FIG.2

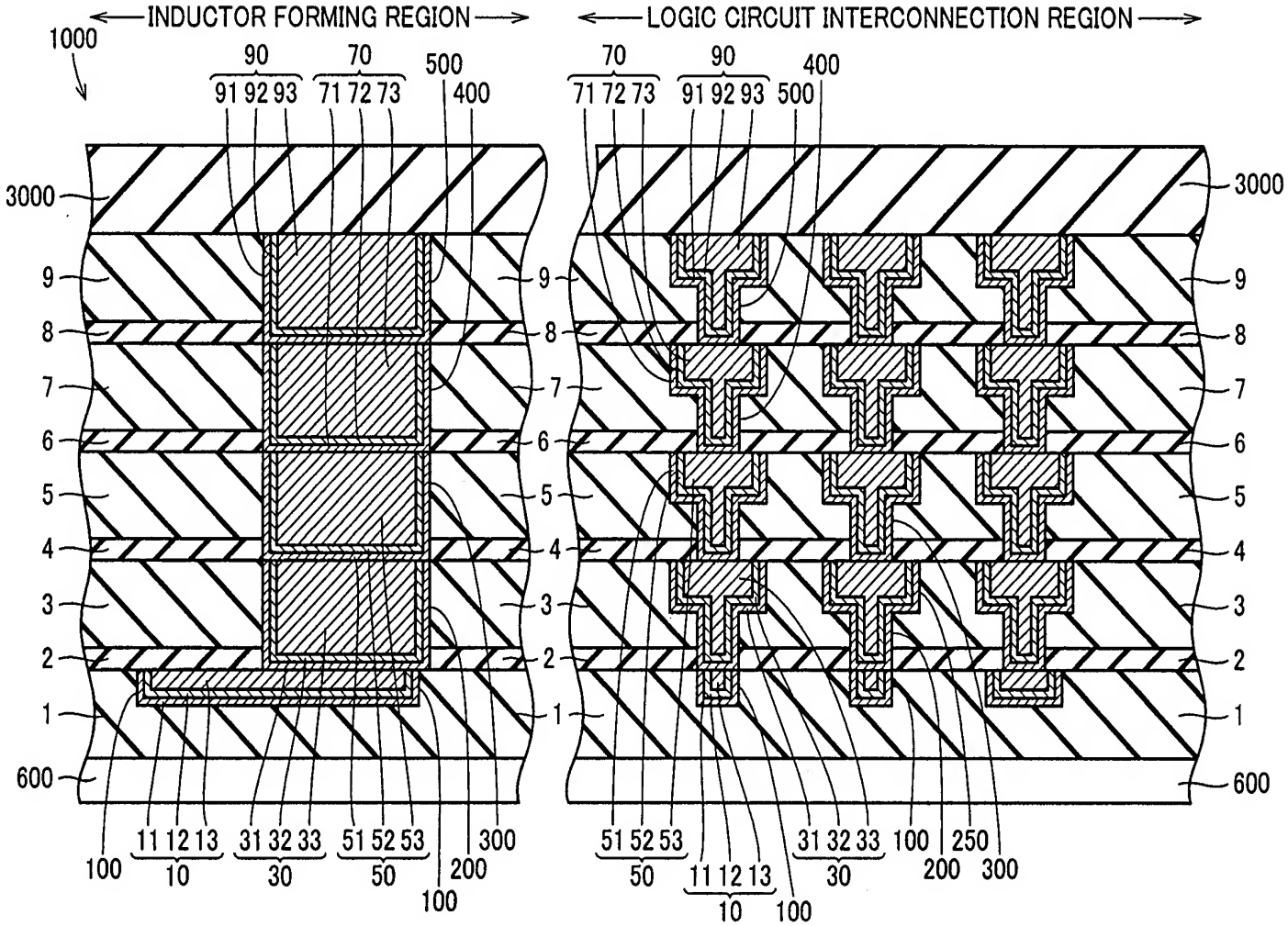
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
1000
90
91 92 93
70
71 72 73
500
400
3000
9
8
7
6
5
4
3
2
1
600
100
11 12 13
10
31 32 33
30
51 52 53
50
300
200
250

FIG.3

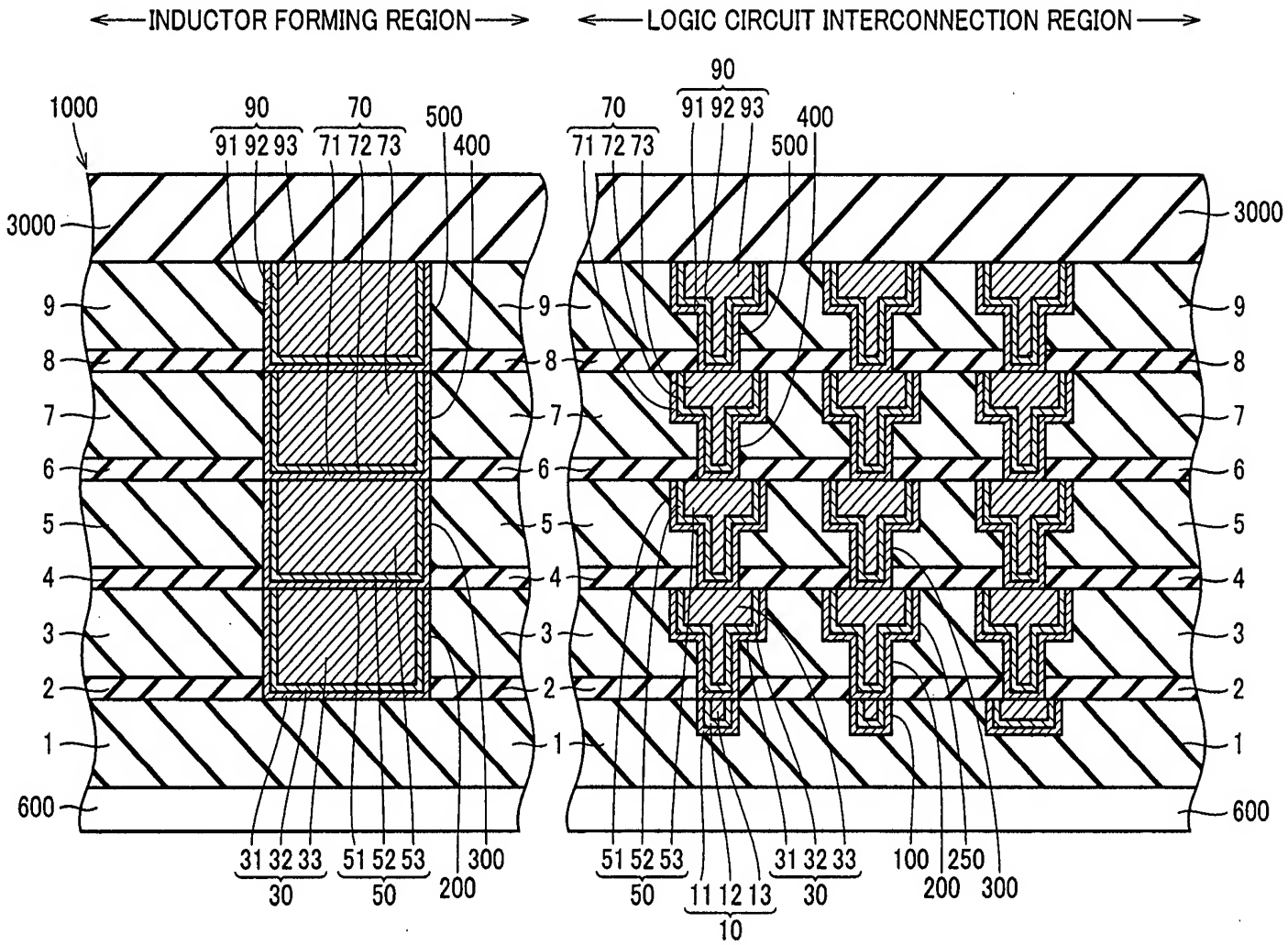
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
1000
90
91 92 93
70
71 72 73
500
400
3000
9
8
7
6
5
4
3
2
1
600
31 32 33
30
51 52 53
50
300
200
11 12 13
10
100
250

FIG.4

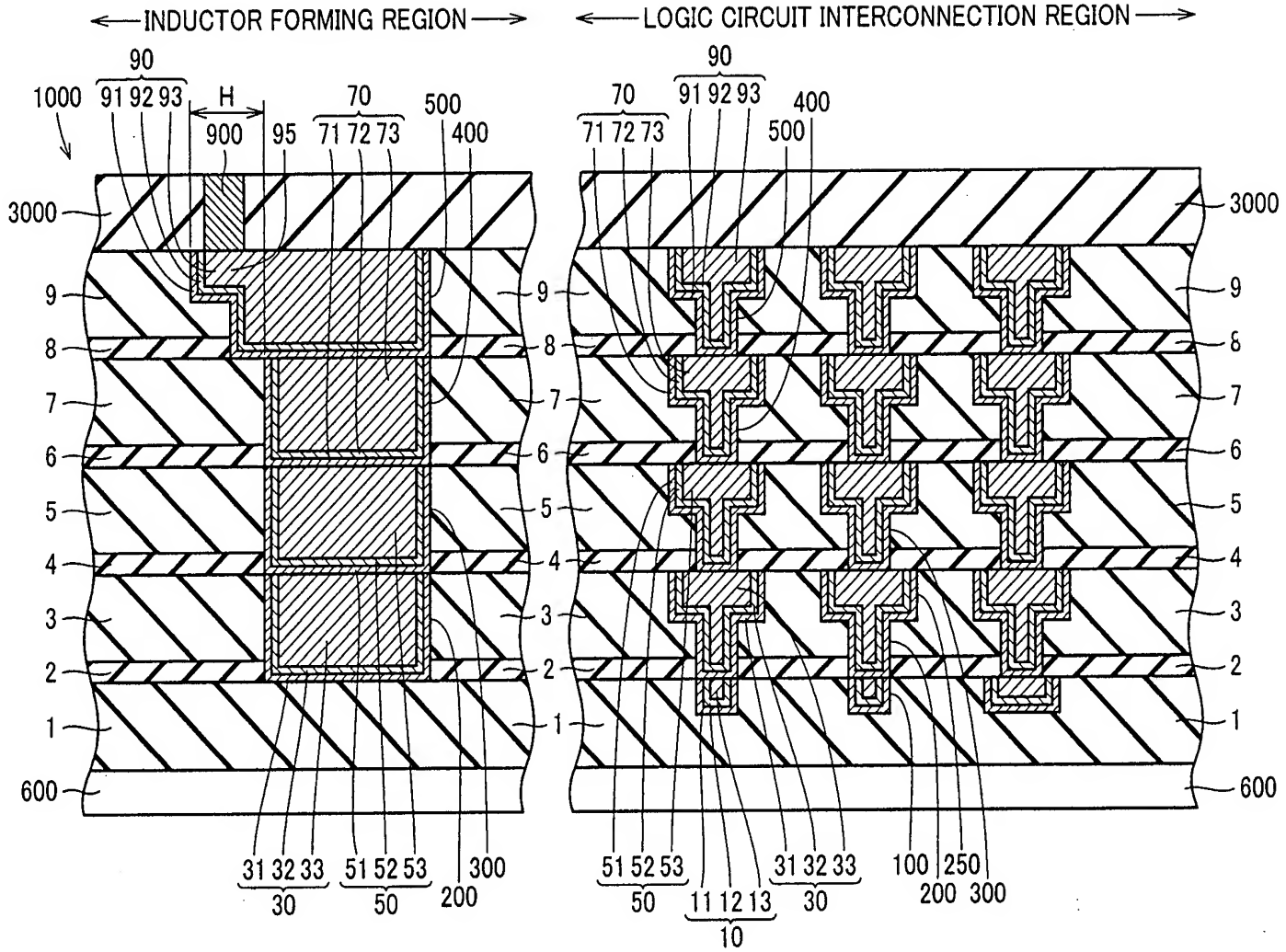
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
1000
90
91 92 93
H
900
95
70
71 72 73
500
400
3000
9
8
7
6
5
4
3
2
1
600
31 32 33
30
51 52 53
50
300
200
11 12 13
10
100
250

FIG.5

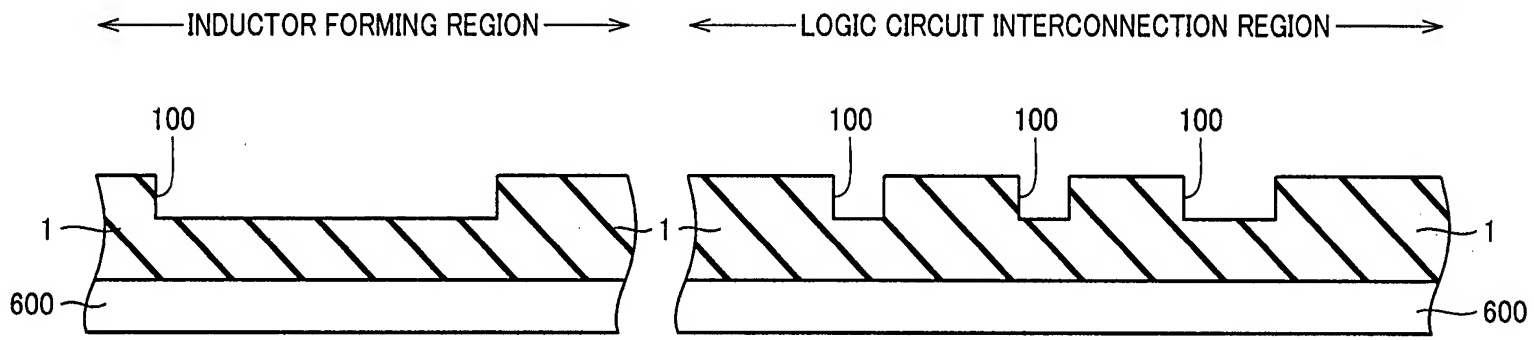
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
100
100
100
100
1
1
1
600
600

FIG.6

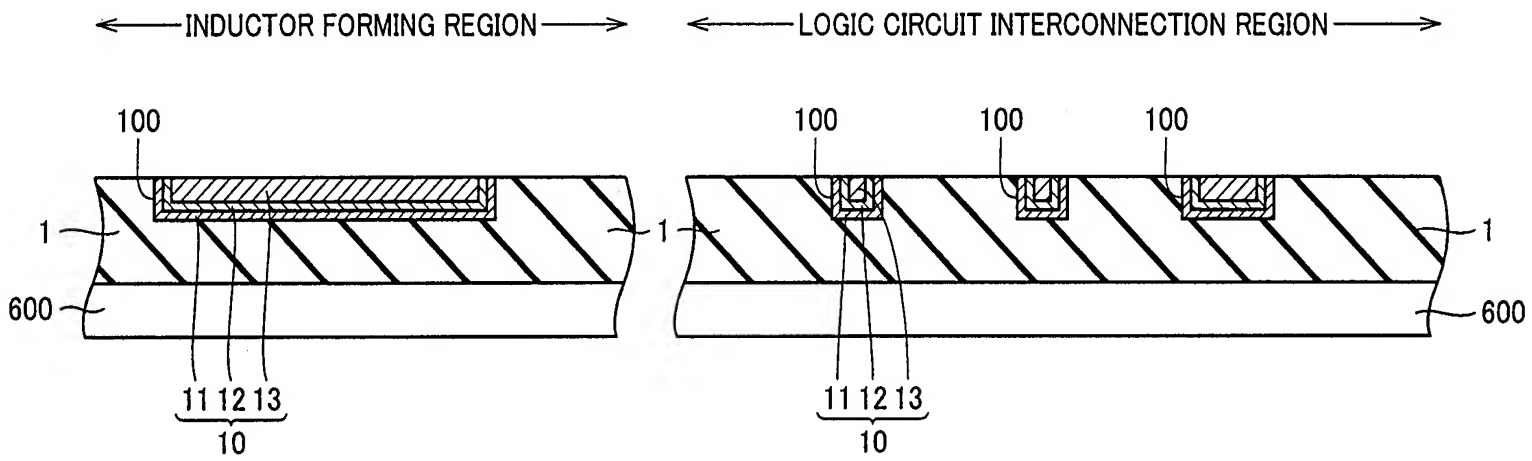
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
100
100
100
100
1
1
1
600
600
11 12 13
10
11 12 13
10

FIG.7

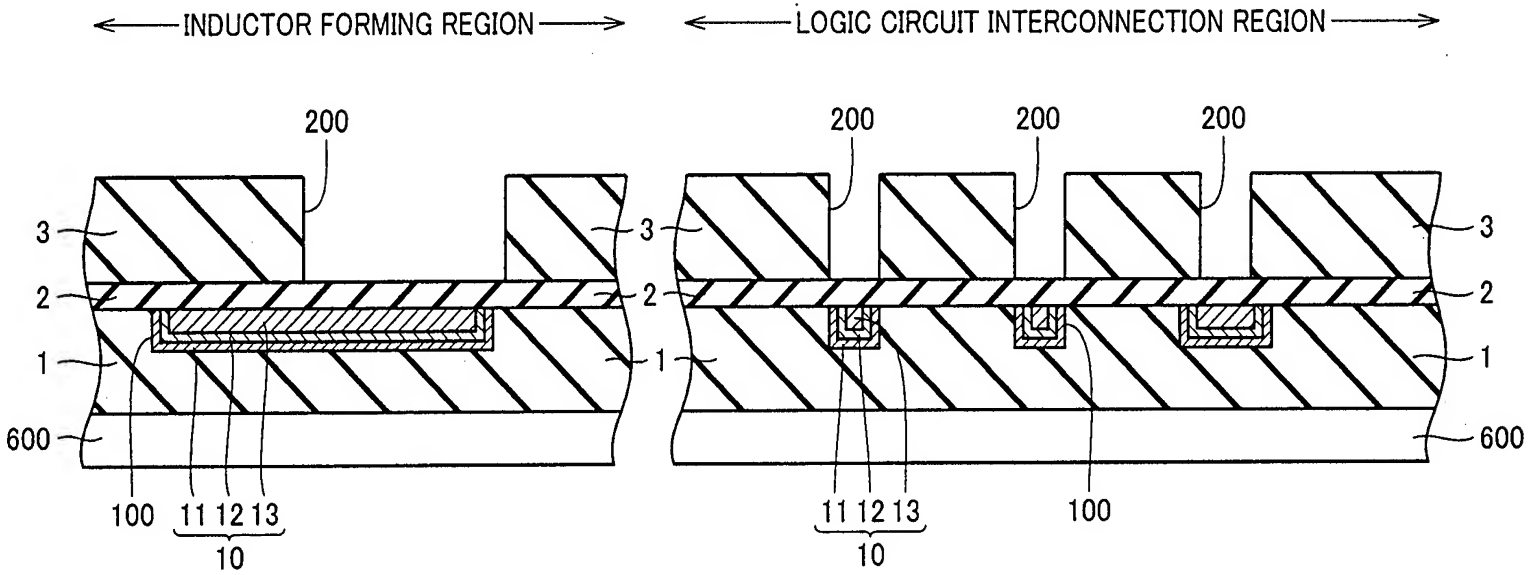
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
200
200
200
200
3
3
3
2
2
2
1
1
1
600
600
100
11 12 13
10
11 12 13
10
100

FIG.8

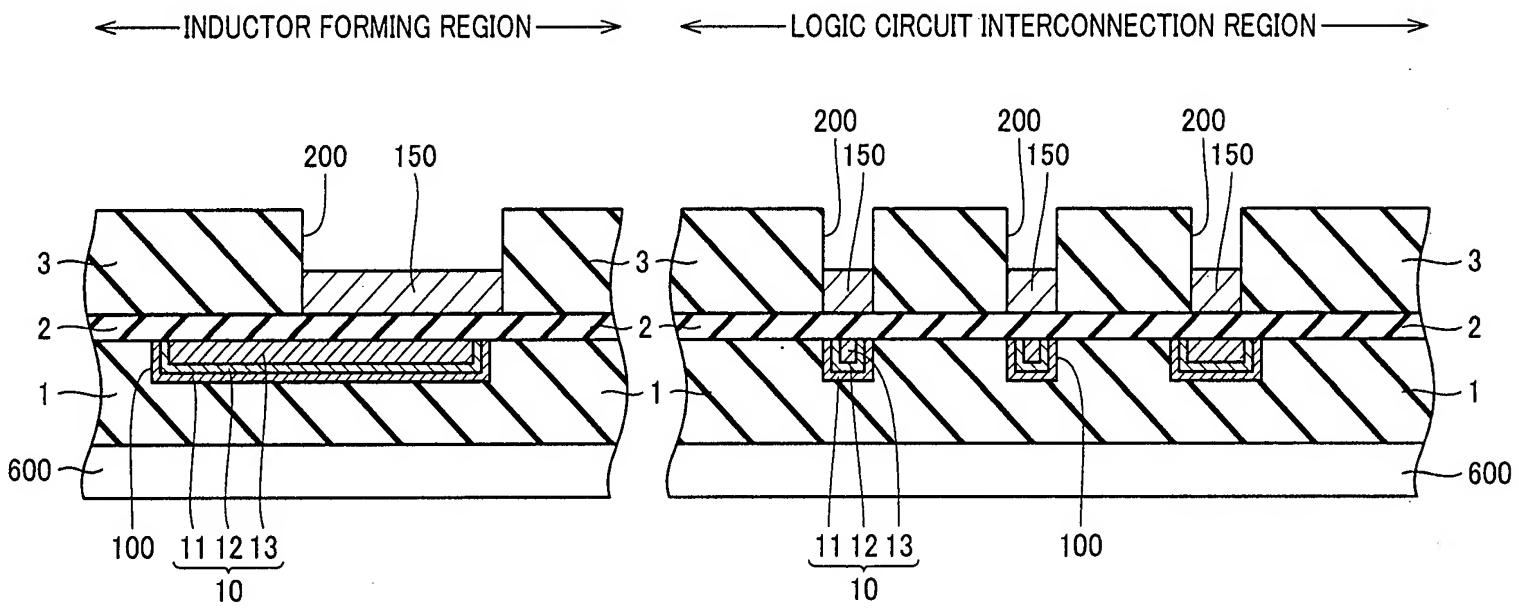
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
200
150
3
2
1
600
100
11 12 13
10

FIG.9

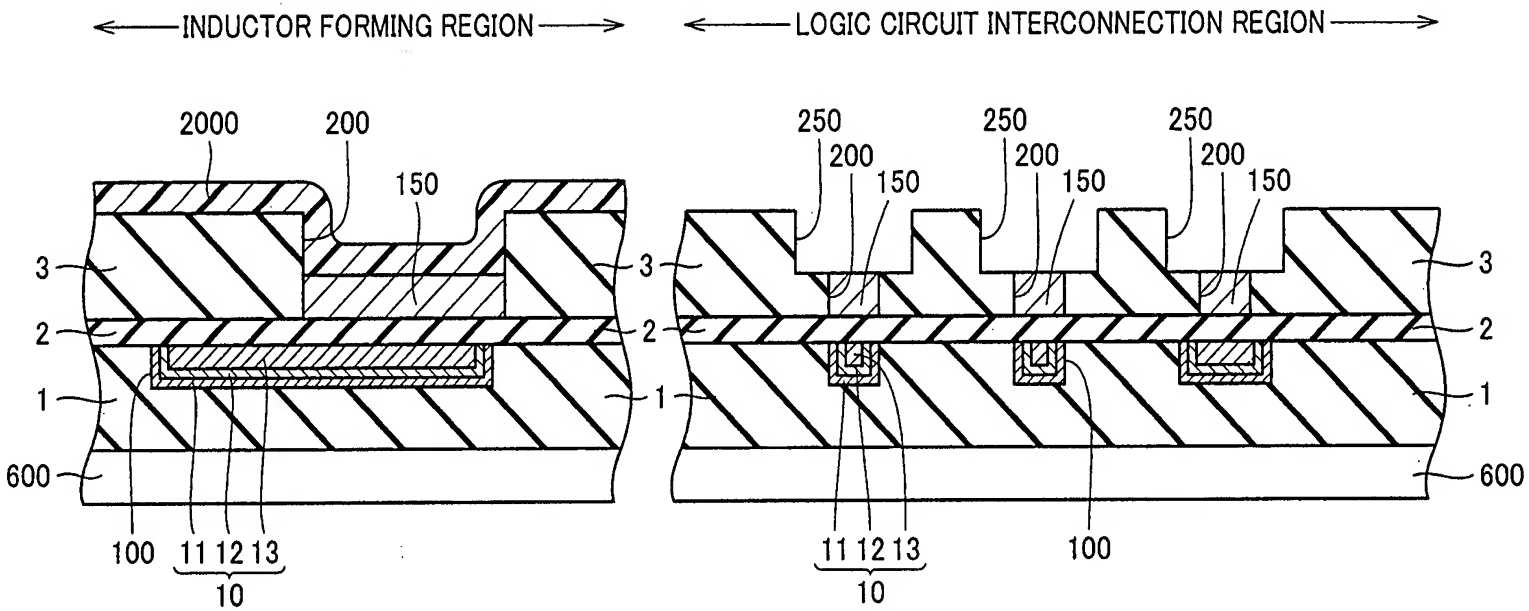
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
2000
200
150
250
250
250
200
200
200
150
150
150
3
2
1
600
100
11 12 13
10

FIG.10

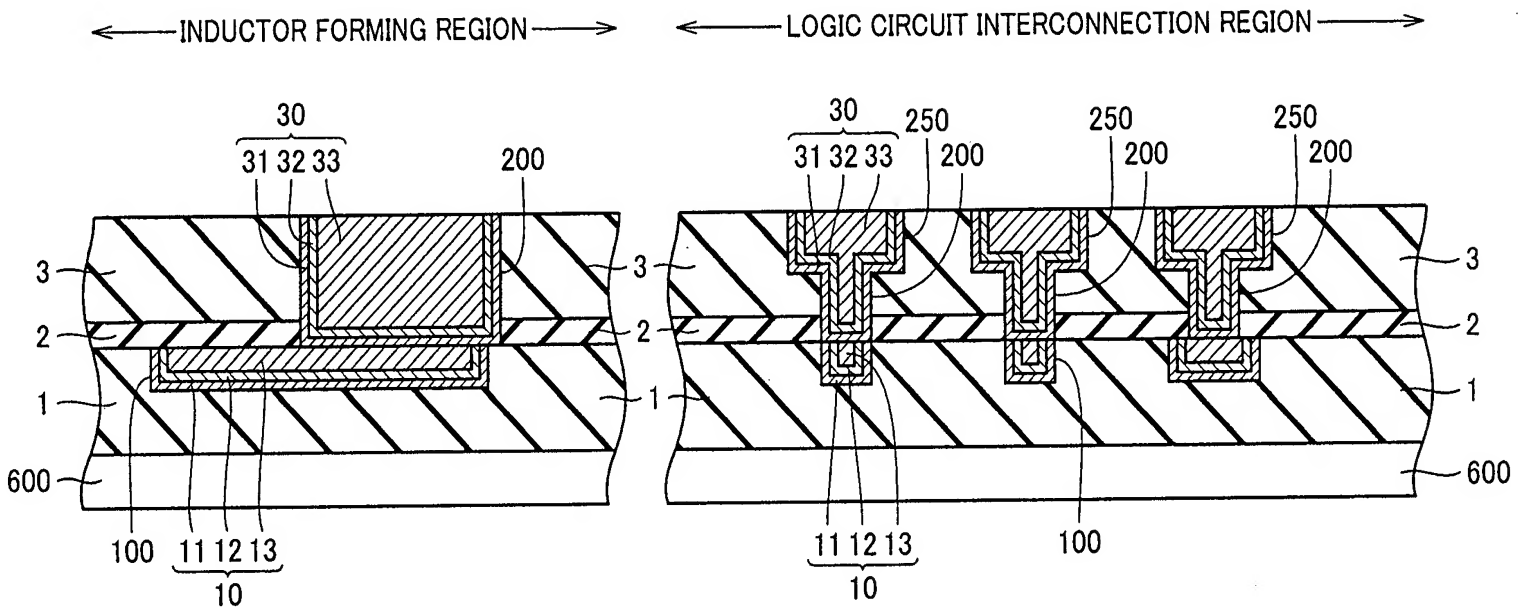
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
30
31 32 33
200
250
3
2
1
600
100
11 12 13
10

FIG.11

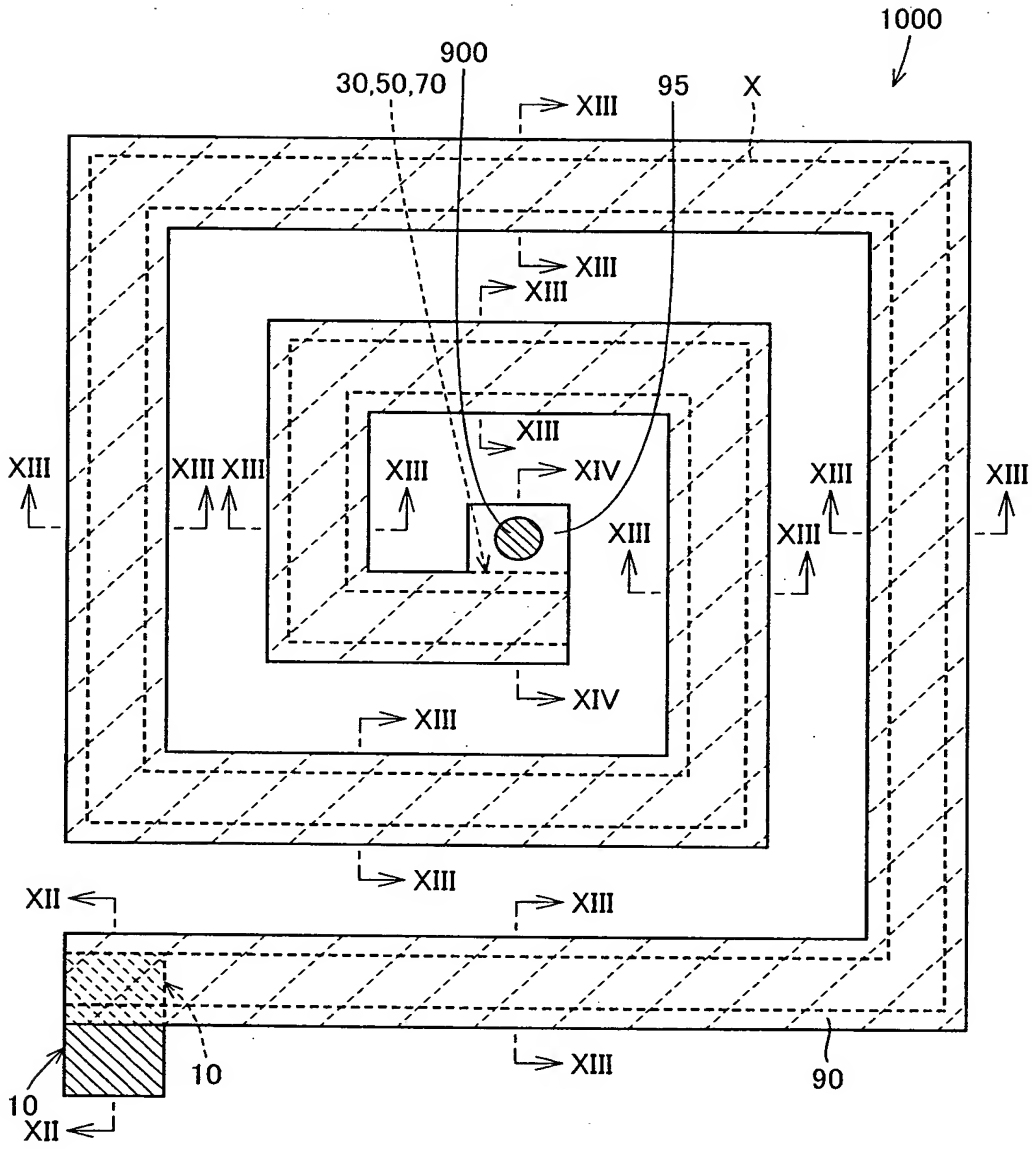

FIG.12

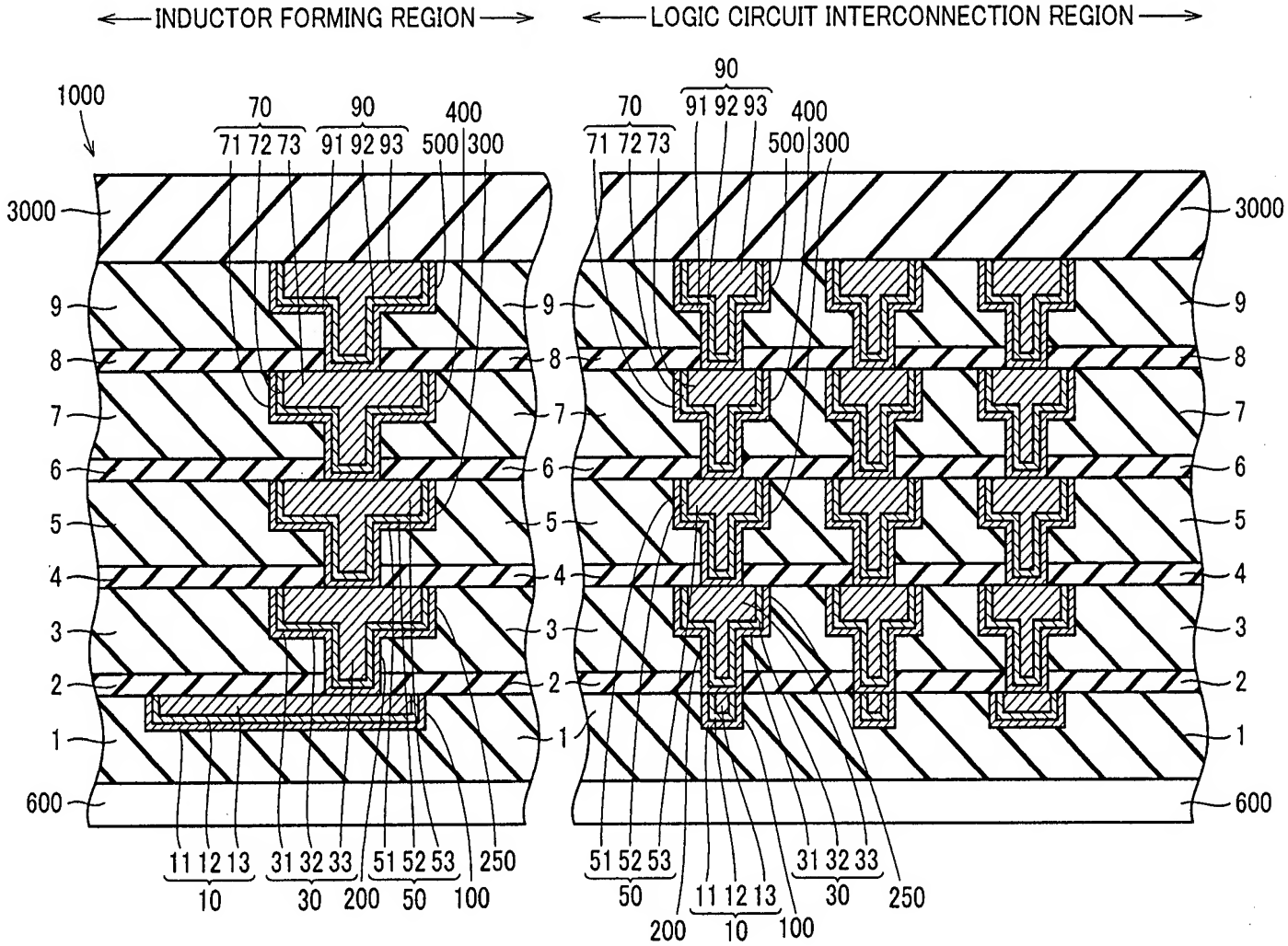
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
1000
70
71 72 73
90
91 92 93
400
500
300
3000
9
8
7
6
5
4
3
2
1
600
11 12 13
10
31 32 33
30
200
51 52 53
50
100
250

FIG.13

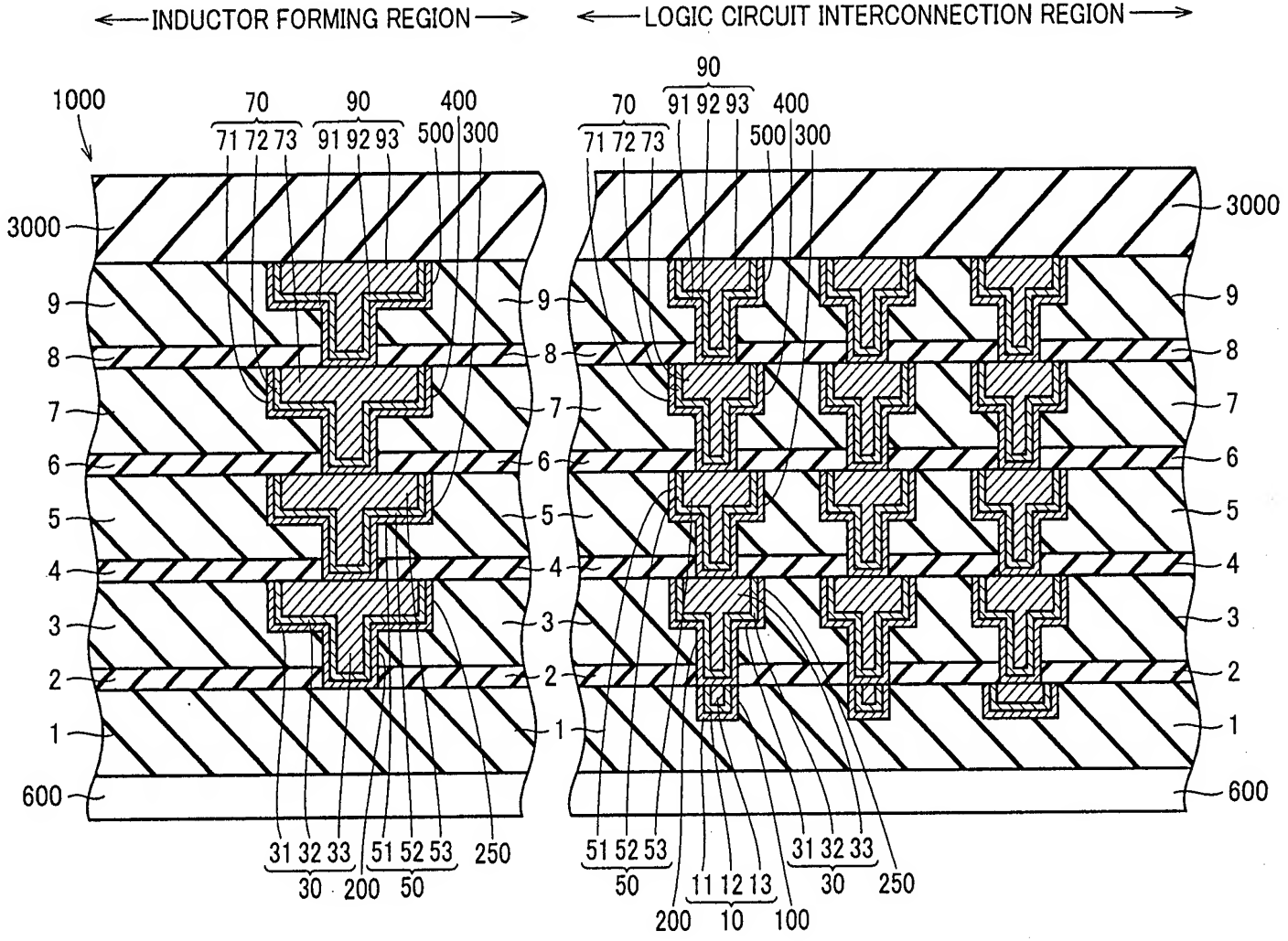
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
1000
70
71 72 73
90
91 92 93
400
500
300
3000
9
8
7
6
5
4
3
2
1
600
31 32 33
30
51 52 53
50
200
250
11 12 13
10
100

FIG.14

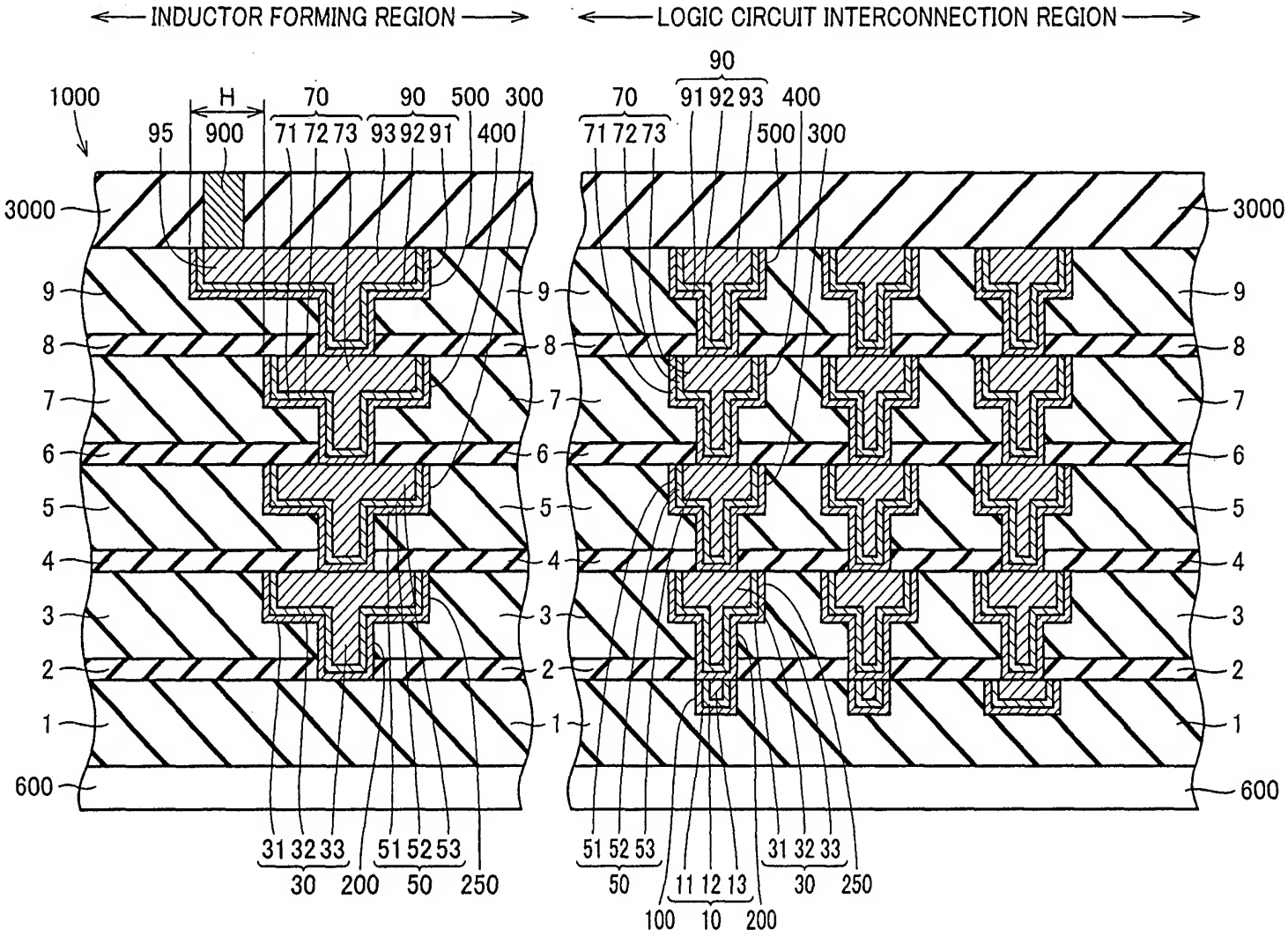
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
1000
H
95
900
71 72 73
70
93 92 91
90
500
400
300
91 92 93
3000
9
8
7
6
5
4
3
2
1
600
31 32 33
30
200
51 52 53
50
250
11 12 13
100
10

FIG.15

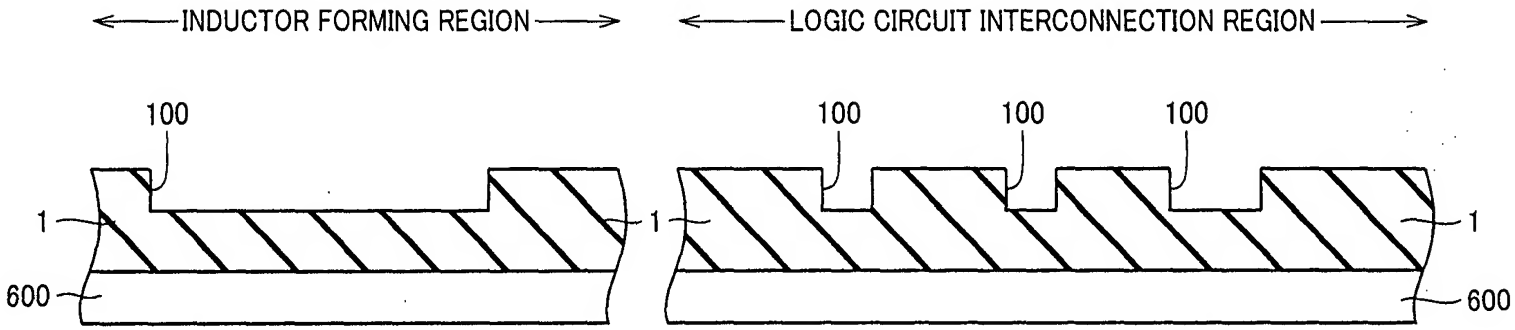
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
100
100
100
100
1
1
1
600
600

FIG.16

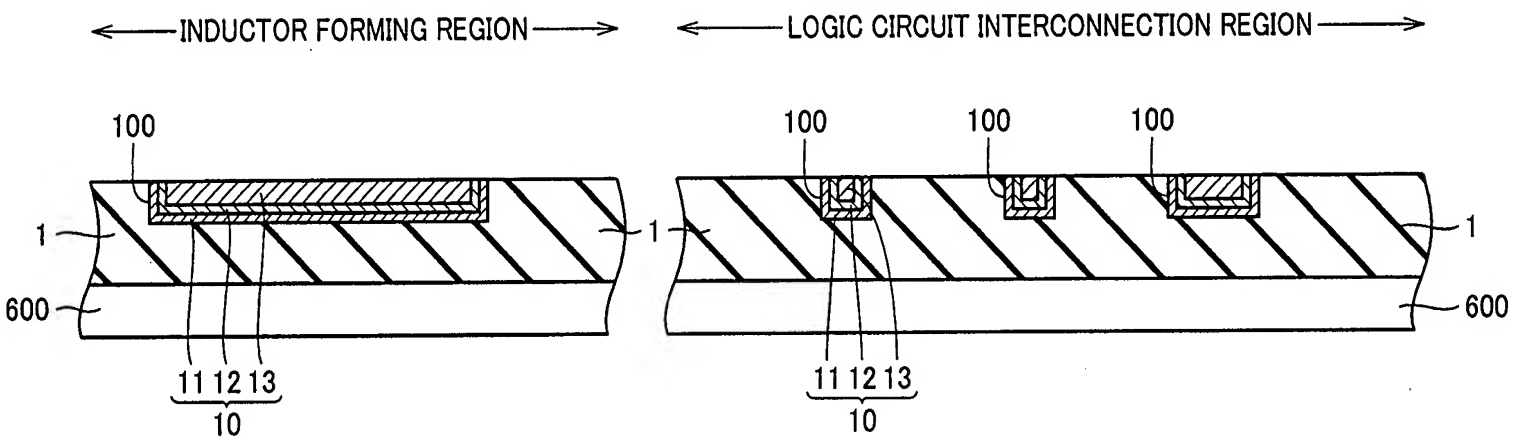
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
100
100
100
100
1
1
1
600
600
11 12 13
10
11 12 13
10

FIG.17

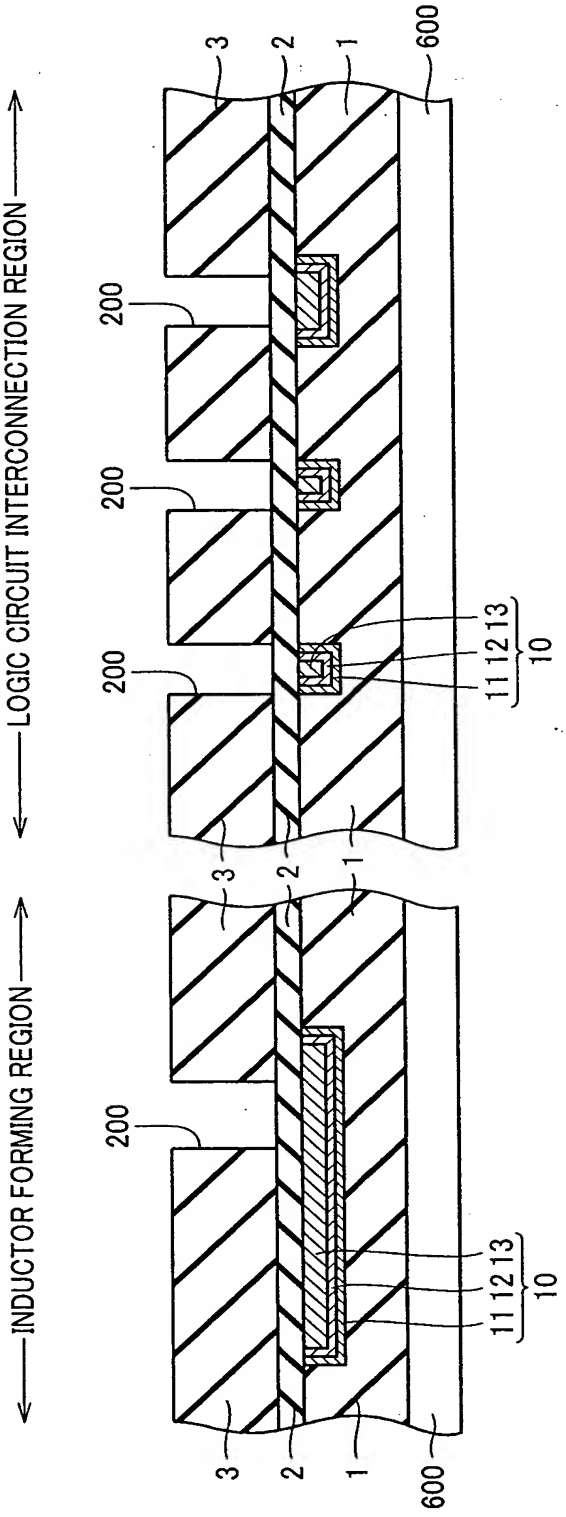
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
200
200
200
200
3
2
1
600
11 12 13
10

FIG.18

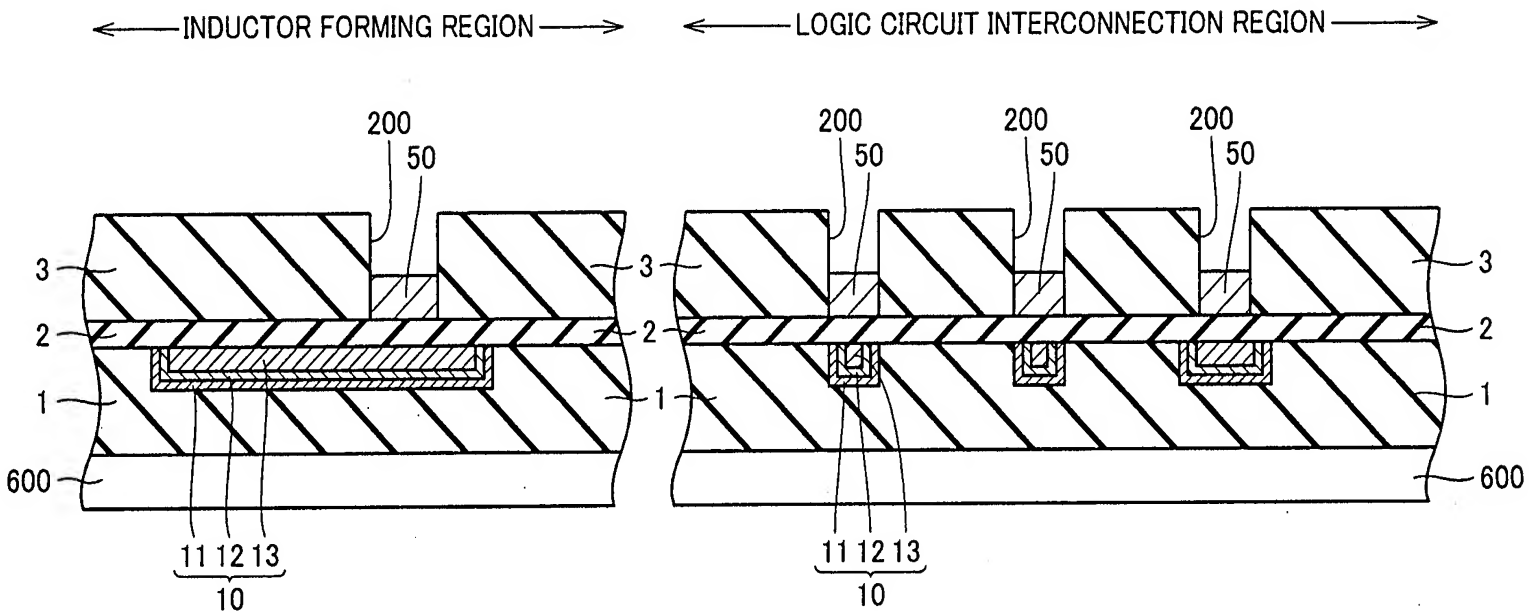
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
200
50
3
2
1
600
11 12 13
10

FIG.19

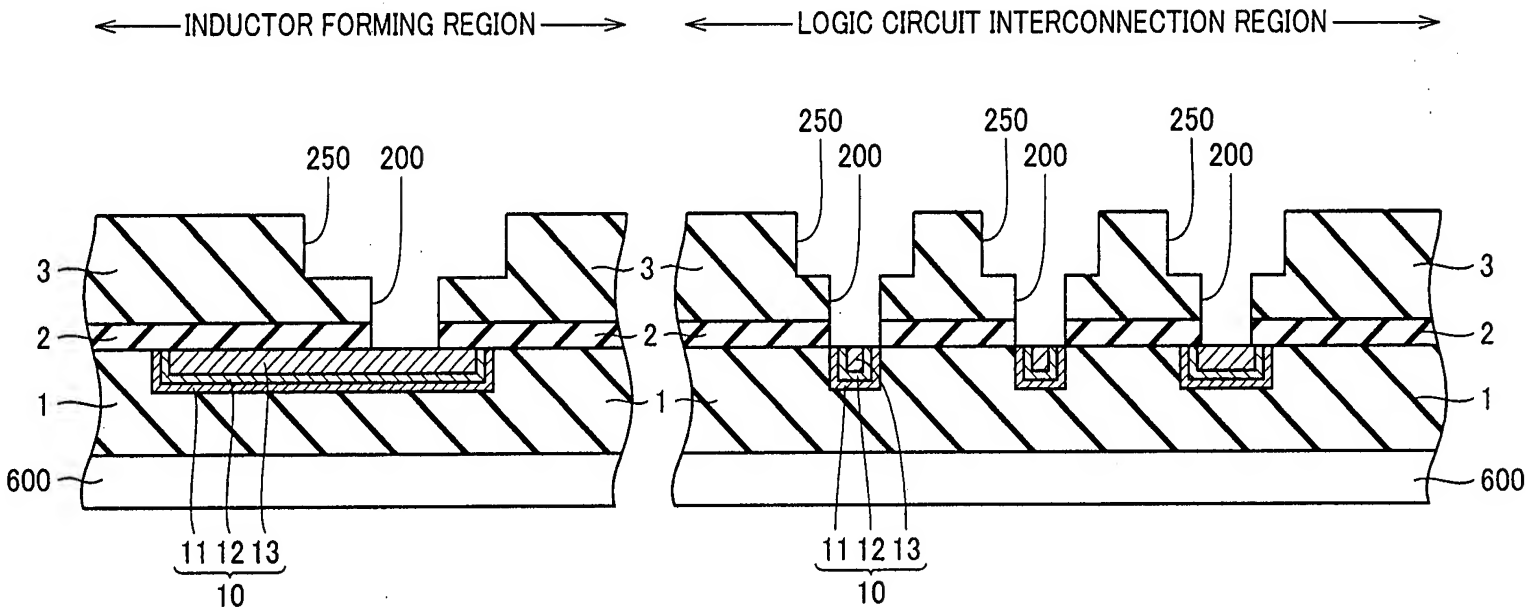
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
250
200
3
2
1
600
11 12 13
10

FIG.20

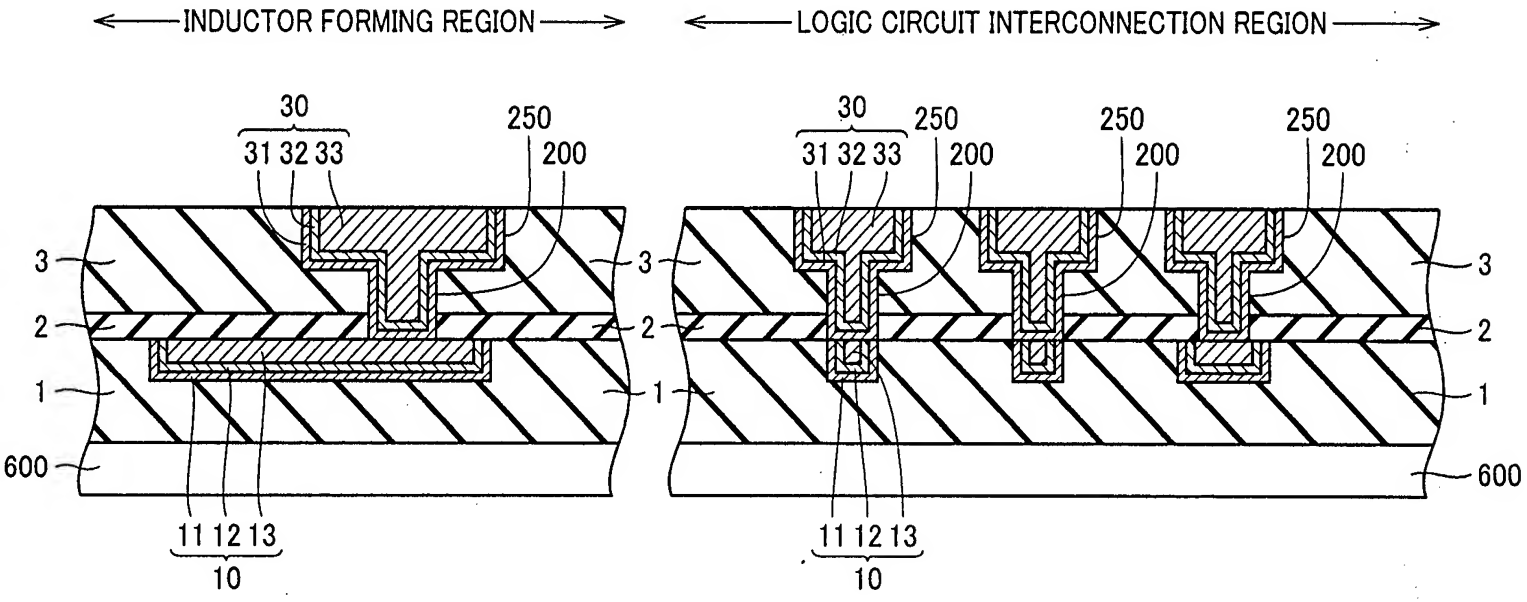
INDUCTOR FORMING REGION
LOGIC CIRCUIT INTERCONNECTION REGION
30
31 32 33
250
200
3
2
1
600
11 12 13
10

FIG.21